What is claimed is:

1. A method of decomposing timing jitter on a signal under test (SUT) comprising an arbitrary serial data stream, said method comprising:

forming a group of measurements, where each measurement comprises a timing jitter value and an associated bit pattern representing the bits falling within an analysis window of a chosen length, said window being successively located at a plurality of positions within the SUT; and

performing a statistical analysis on said group of measurements to calculate the mean value of the inter-symbol interference (ISI) associated with each bit pattern.

2. The method of claim 1, wherein said ISI jitter is determined for a specified edge polarity only.

3. The method of claim 1, further comprising separating random and periodic jitter.

4. The method of claim 1, further comprising estimating duty cycle distortion (DCD).

5. The method of claim 4, further comprising removing said DCD from a record.

6. The method of claim 4, further comprising estimating the probability density function (PDF) of said ISI plus said DCD.

7. The method of claim 1, further comprising removing said ISI from a record.

8. The method of claim 1, further comprising estimating the probability density function (PDF) of said ISI.

9. A test and measurement device, comprising:

an acquisition module, for acquiring a first SUT to produce a first sample stream;

a processing module, for

forming a group of measurements, where each measurement comprises a timing jitter value and an associated bit pattern representing the bits falling within an analysis window of a chosen length, said window being successively located at a plurality of positions within the SUT, and

performing a statistical analysis on said group of measurements to calculate the mean value of the inter-symbol interference (ISI) associated with each bit pattern; and

a display module, for displaying results of said statistical analysis.

10. The test and measurement device of claim 9, wherein said processing module is further for determining said ISI jitter for a specified edge polarity only.

11. The test and measurement device of claim 9, wherein said processing module is further for separating random and periodic jitter.

12. The test and measurement device of claim 9, wherein said processing module is further for estimating duty cycle distortion (DCD).

13. The test and measurement device of claim 9, wherein said processing module is further for removing said DCD from a record.

14. The test and measurement device of claim 9, wherein said processing module is further for removing said ISI from a record.

15. A computer-readable media for storing software instructions which when executed by a processor perform the steps of:

decomposing timing jitter on a signal under test (SUT) comprising an arbitrary serial data stream, by

forming a group of measurements, where each measurement comprises a timing jitter value and an associated bit pattern representing the bits falling within an analysis window of a chosen length, said window being successively located at a plurality of positions within the SUT; and

performing a statistical analysis on said group of measurements to calculate the mean value of the inter-symbol interference (ISI) associated with each bit pattern.

16. The computer-readable media of claim 15, wherein said ISI jitter is determined for a specified edge polarity only.

17. The computer-readable media of claim 15, further comprising instructions for separating random and periodic jitter.

18. The computer-readable media of claim 15, further comprising instructions for estimating duty cycle distortion (DCD).

19. The computer-readable media of claim 15, further comprising instructions for removing said DCD from a record.

20. The computer-readable media of claim 15, further comprising instructions for removing said ISI from a record.